Abstracts

High-Yield Design Technologies for InAlAs/InGaAs/InP-HEMT Analog-Digital ICS

Y. Umeda, T. Enoki, K. Osafune, H. Ito and Y. Ishii. "High-Yield Design Technologies for InAlAs/InGaAs/InP-HEMT Analog-Digital ICS." 1996 Transactions on Microwave Theory and Techniques 44.12 (Dec. 1996, Part II [T-MTT] (1996 Symposium Issue)): 2361-2368.

Sixty-GHz-band two-stage monolithic low-noise amplifiers and ultrahigh-speed SCFL static frequency dividers have been fabricated using the same InAIAs/InGaAs/fnP HEMT process. This process assures uniformity by taking advantage of a O.1-µm T-shaped gate and an InP recess-etch stopper. Circuits are designed with priorities on stable operation, high yield, and uniformity. For the low-noise amplifier, the stabilization is optimized so as to minimize noise for the design gain while maintaining stability at all frequencies. The resultant amplifiers show a fabrication yield of 75% and at 62 GHz have a noise figure of 4.3 + 0.19 dB and a gain of 11.8 ± 0.25 dB. For the frequency divider, the load resistance is set to be large enough to assure stable operation (circuit simulation shows that increasing the load resistance has little effect on the maximum toggle frequency). Frequency dividers designed with the optimum load resistance for stable and high-speed operation show a fabrication yield of 63% and have a maximum toggle frequency of 36.7 ± 0.55 GHz. These results demonstrate the feasibility of using this HEMT process to monolithically integrate analog and digital circuits on one chip.

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